

Crosstalk Minimization in VLSI Interconnects

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ABSTRACT

Crosstalk noise is often induced in long interconnects running parallel to each other. There arises a need to minimize the effect of these crosstalk noise so as to maintain the signal integrity in interconnects. So in this paper crosstalk noise is minimized using various techniques such as repeater (bidirectional buffer) insertion along with shielding, skewing and shielding & skewing simultaneously. With the help of these techniques crosstalk noise is controlled to a great extent in long interconnects. Prelayout simulations for crosstalk are carried out for different techniques at 90nm technology nodes using cadence. The influences of these techniques are analyzed and it is found that crosstalk is reduced upto 57%.

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1. INTRODUCTION

In today's era of technology miniaturization of devices is highly responsible for the growth of VLSI circuits. As the technology is scaling more and more number of devices is organized on chips causing the requirement of large number of interconnects [1]. These interconnects associate parasitic along with it which are responsible to degrade the signal waveforms. In submicron technologies various design techniques causes increase in coupling effects in interconnects [4]. Due to these capacitive couplings there is noise induced sometimes to great extent that one cannot ignore the noise effects on signal. The noise is referred to as crosstalk noise. Crosstalk noise is the undesired form of energy that is imparted to various interconnects models due to signal propagation in adjacent lines. Generally crosstalk has two major impacts on the behavior of circuits such as it induces delay which might change the propagation time of the circuit or may cause voltage spikes resulting in degradation of the signal. Dynamic crosstalk occurs due to simultaneous switching of adjacent lines in opposite or in same phase. There are various techniques which can be used to reduce the effect of crosstalk in interconnects such as repeater insertion, shielding and skewing.

1.1. Repeater Insertion

Repeater insertion is technique used basically to maintain the signal strength in long interconnects [1]. As we know in long interconnects various factors can degrade the signal performance so there is much need of repeater insertion. Repeaters are capable of reducing the time delays associated with long interconnect in VLSI circuits [1]. As the time delay is reduced and the moreover signal is restored after each repeater the crosstalk is also reduced after signal restoration at repeater node.

1.2. Shielding

In high speed digital circuits Shielding is an effective and common way to reduce crosstalk noise and signal delay uncertainty [2]. Even in a 600MHz Alpha microprocessor, two entire layers of metal are dedicated for shielding [3]. A universal method of shielding is placing ground or power lines at the sides of a

victim signal line to reduce noise and delay uncertainty. The crosstalk between two coupled interconnects is often neglected when a shield is inserted, significantly underestimating the coupling noise.

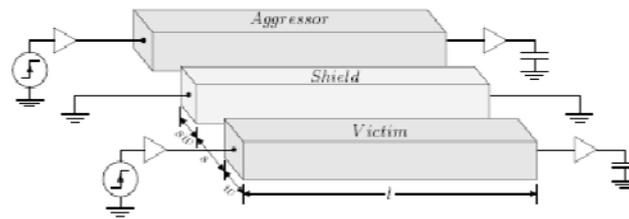


Figure 1. Shielding in interconnects

1.3. Skewing

The maximum propagation delay and crosstalk noise occurred when the drivers were switching in opposite directions as compared to drivers switching in same direction [4]. Skewing is nothing but static delay introduced in signal propagation. Thus the skewing of drivers caused the reduction in time in switching of drivers thereby reducing the crosstalk.

1.4. Skewing & Shielding

Individually skewing and shielding leads to reduction in crosstalk. Also when both these techniques are employed simultaneously crosstalk is reduced.

2. RELATED WORK

Gargi Khanna et al. [3] analyzed crosstalk induced influences on interconnects power dissipation, delay, undershoot and overshoot noise caused by terminating load variations in adjacent lines. In one element capacitive load is varied and in other aggressor line fanout is varied. A terminating load adjustment can achieve some control over crosstalk.

Kaushik et al. [4] studied the crosstalk noise due to presence of self and mutual parasitic inductance and capacitance. An interpretation is drawn from simulation results that in the worst case of an overshoot or undershoot, false switching and/or gate oxide wear out can occur which may result in malfunctioning of the chip. Such noise may cause an erroneous value to be stored in latches/flip-flops. It has been argued by others that inductance induced problems are most pronounced in long buses, and that there is no need to study such noise in medium length interconnects. It is observed that, in current technology, interconnects in semi global lengths are long enough to give rise to significant crosstalk induced errors. Therefore, inductance induced noise should be considered during test generation for combinational blocks with medium length lines.

Meindl et al. [5] derived the compact expressions that describe the transient response of distributed coupled interconnects including worst-case time delay and crosstalk. These new expressions enhance understanding and computation of inductive effects in a GSI multilevel network. For a 3GHz global die-edge length interconnect, the inclusion of inductance 1) increases worst-case peak crosstalk over 60%; 2) requires an increase in the wiring spacing over 40%; 3) introduces a new nonlinear length dependence of peak crosstalk voltage that has a peak that can be up to 1.57 larger than the predicted value; 4) reveals the dependence of inductive crosstalk on driver impedance. Finally, a new closed-form expression for the peak crosstalk voltage on distributed lines is rigorously derived, and it reveals a coupling length at which the maximum peak crosstalk occurs.

Zhang et al. [6] developed an analytic model of the peak noise based on a pseudo $2\pi RC$ model. A design methodology for inserting shields between coupled interconnects to reduce crosstalk noise is presented.

Eidler et al. [7] investigated power dissipation in CMOS inverters and repeaters driving RC loads. A closed form analytic expression for short-circuit power in a CMOS inverter driving an RC load is presented. In the region of interest, this expression exhibits a maximum error of 15% as compared to SPICE. It is also shown that short-circuit power can represent up to 20% of the total dynamic power dissipation. An empirical comparison of power in repeater chains is presented.

Veleineis et al. [8] developed an algorithm which is applied to a set of interconnect tree structures in order to evaluate the effect of the proposed path-and-branch shielding methodology on the signal delay variations at a critical tree node. The proposed approach is compared with an alternative shielding technique where shielding is applied only along the direct path between the critical node and the signal source. The developed shielding application algorithm is modified in order to implement the alternative method, by advancing the shielding frontier only along the direct path from the critical node to the tree source. For both methodologies, limited shielding resources are considered.

3. PRESENT WORK

In this RLC interconnect model as in Figure 1 is used to study the effect of crosstalk. RLC parameter values are obtained from ptm models which are as follows: $R= 36.666\text{ohms}$, $L= 1.8358\text{nH}$ and $C=82.932\text{fF}$.

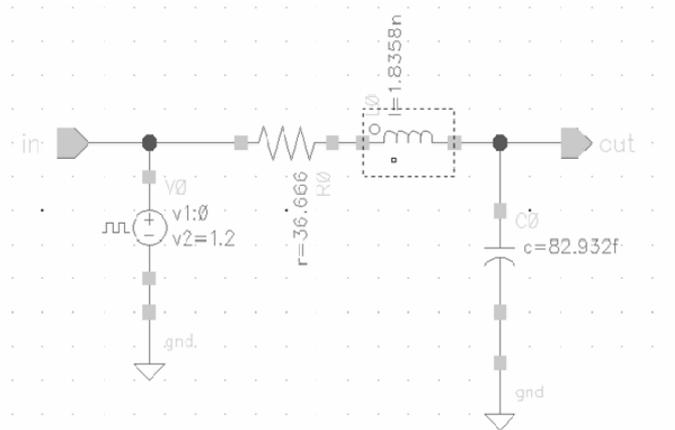


Figure 1. RLC interconnect model

Bidirectional buffer is designed as a repeater in RLC interconnects. This bidirectional buffer is made up of tristate buffers and invertors as shown in Figure 2. Control input pin decides the direction of signal flow.

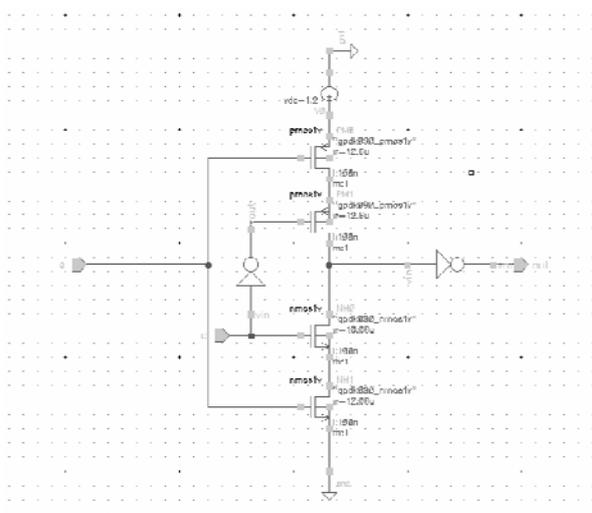


Figure 2. Tristate buffer



Figure 3. Bidirectional buffer

Bidirectional buffer (Figure 3) is designed using tristate buffers and invertors. Input is fed and output is analysed in either direction. Bidirectional buffer symbol is used in various analyses as shown in Figure 4.

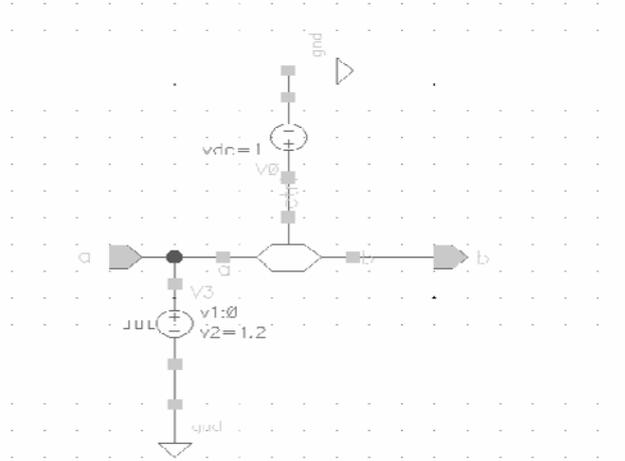


Figure 4. Bidirectional buffer symbol

Thus bidirectional buffer is designed and is implemented as repeater (Figure 5) in RLC interconnects.

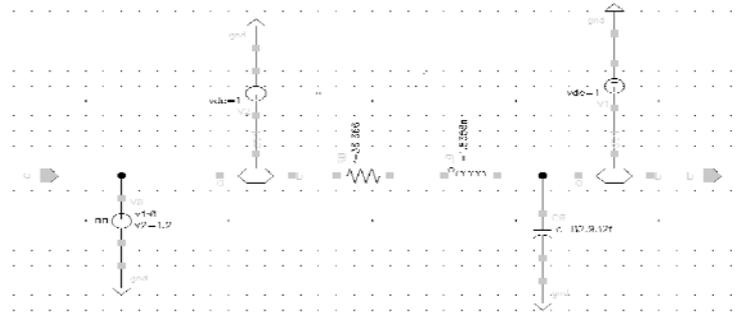


Figure 5. Buffer insertion in RLC interconnects

Analysis of this repeater insertion is done. Two parallel interconnect lines are considered along with coupling capacitances to study the effect of crosstalk in interconnects as in Figure 6. Value of coupling capacitance as per ptm model is chosen to be 88.37fF.

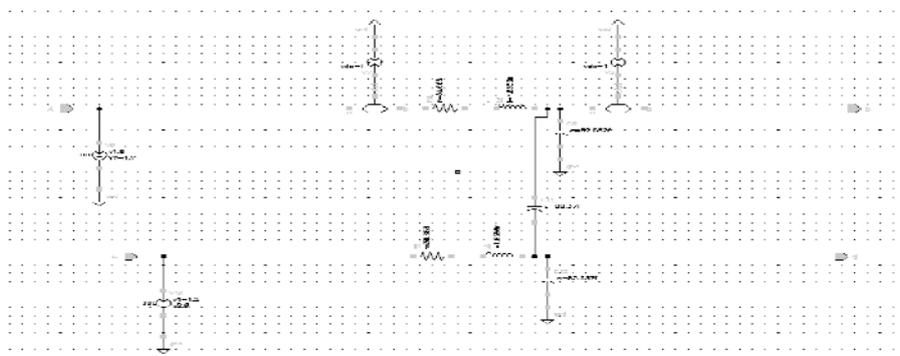


Figure 6. Coupling in interconnects

The dynamic crosstalk is measured with these circuits with voltage sources switching in same and in opposite directions.

Various crosstalk minimization techniques are implemented such as shielding (Figure 7).

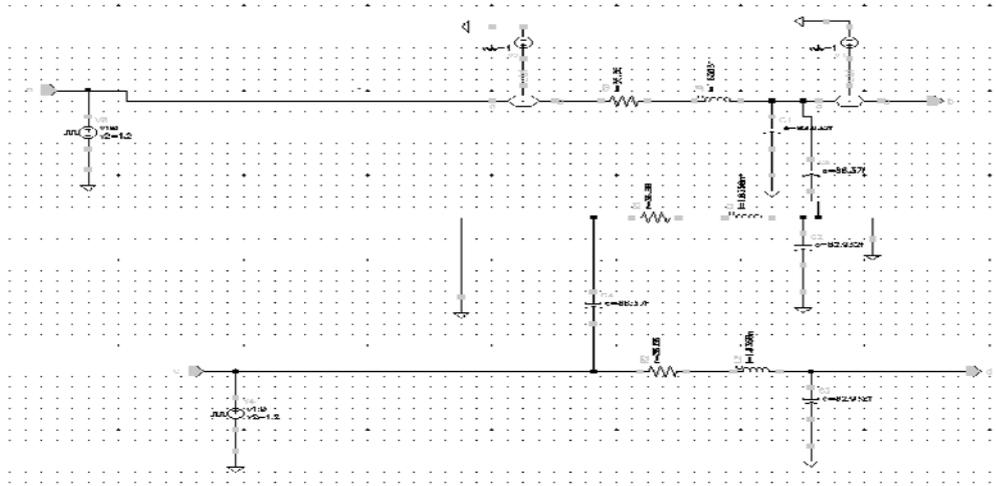


Figure 7. Shielding

Skewing, one of the techniques to reduce crosstalk is also implemented. For introducing skew, delay is inserted using invertors so that there is delay between the switching times of the drivers which may lead to reduction of dynamic crosstalk.

A novel approach to crosstalk reduction is implemented using both skewing and shielding techniques simultaneously as shown in Figure 8. This has minimized crosstalk to great extent.

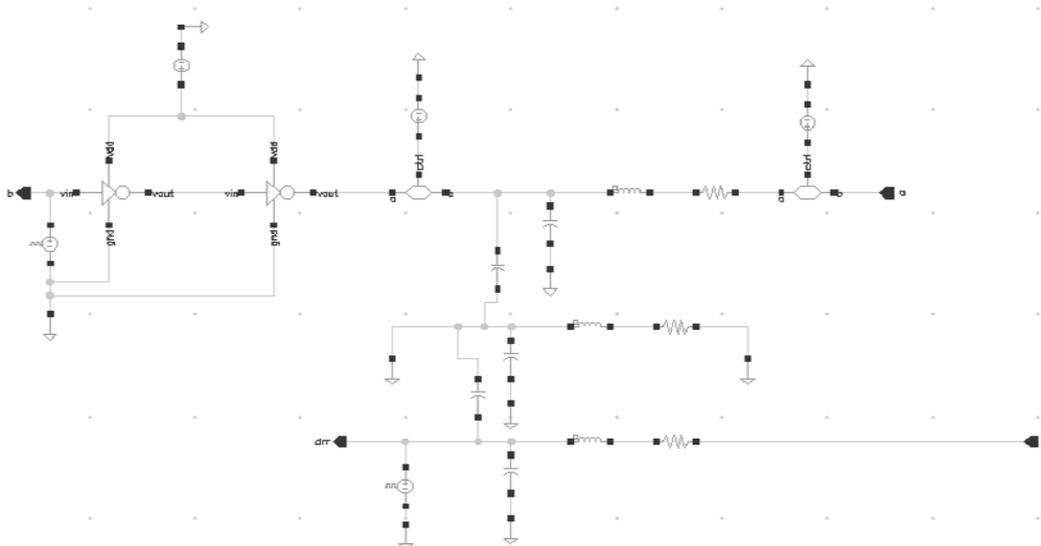


Figure 8. Skewing & Shielding

4. RESULTS AND ANALYSIS

RLC interconnect model analysis has been done and simulation results at 2GHz are shown in Figure 9.

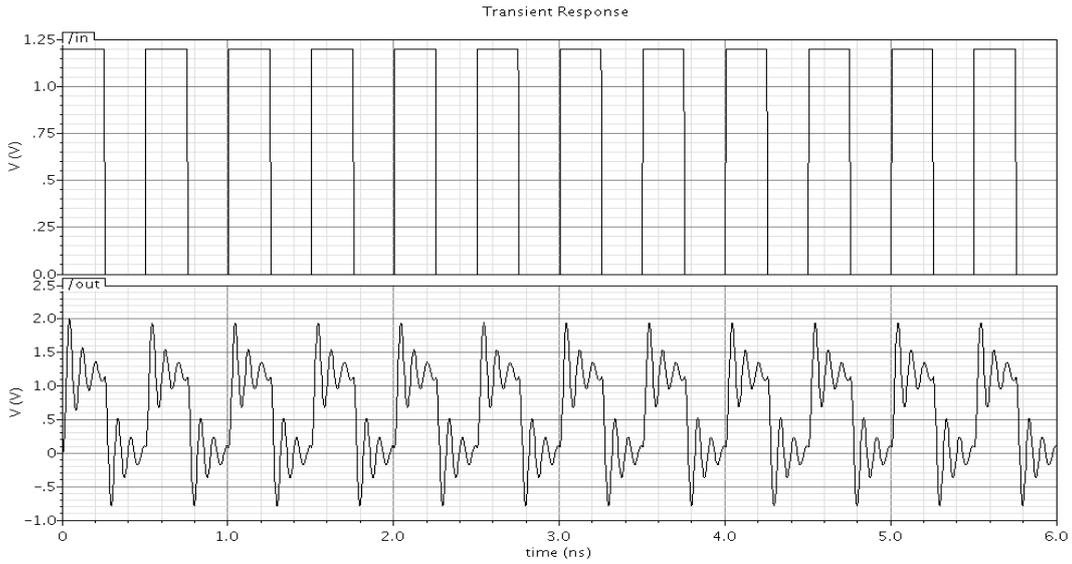


Figure 9. RLC analysis

In Figure 10, 11 Bidirectional Buffer is designed as a repeater at 2GHz in both directions as per input to control signal.

a) When control is high

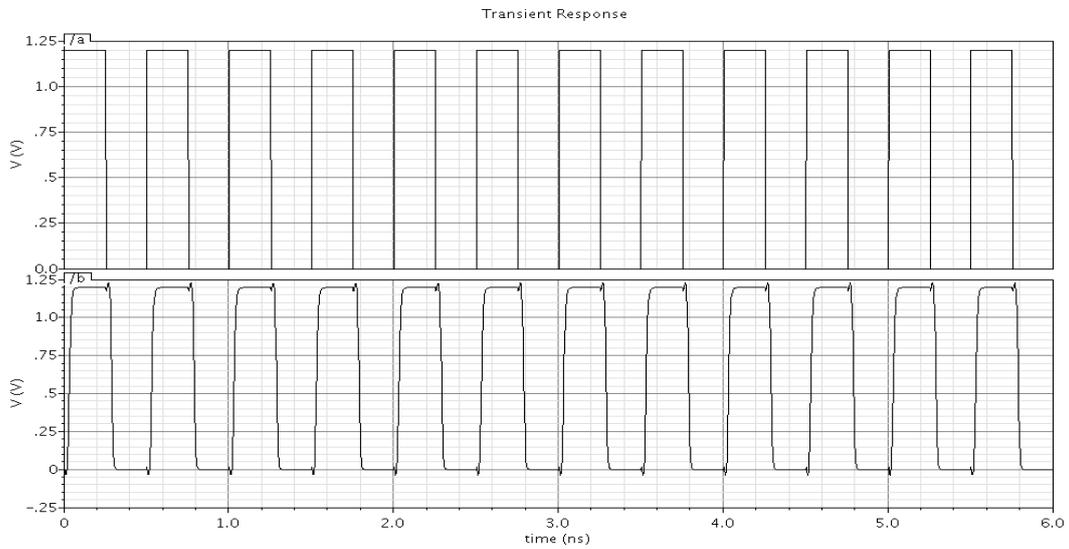


Figure 10. Bidirectional Buffer A to B

b) When control is low

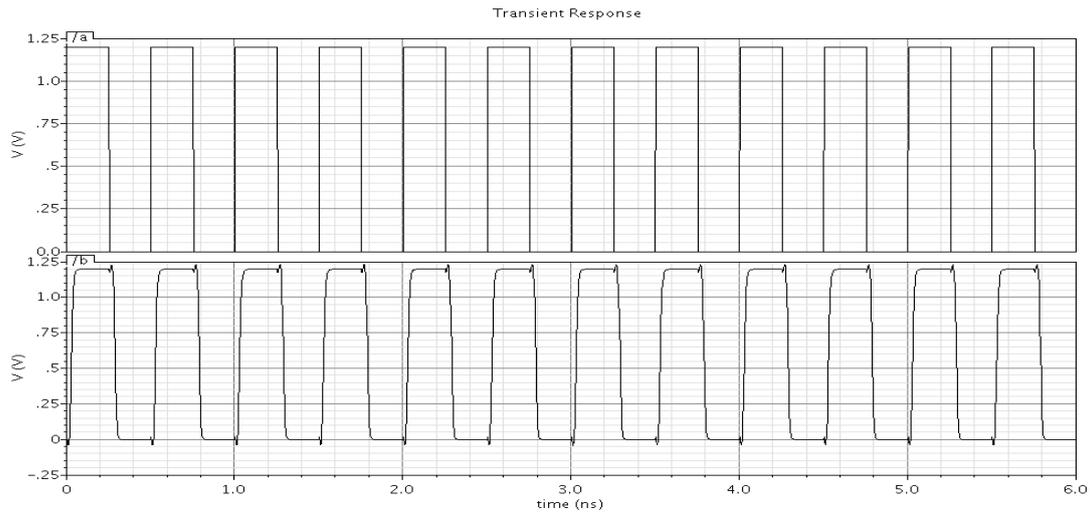


Figure 11. Bidirectional Buffer B to A

Now this bidirectional buffer is inserted in RLC interconnect model. Transient analysis obtained is as in Figure 12.

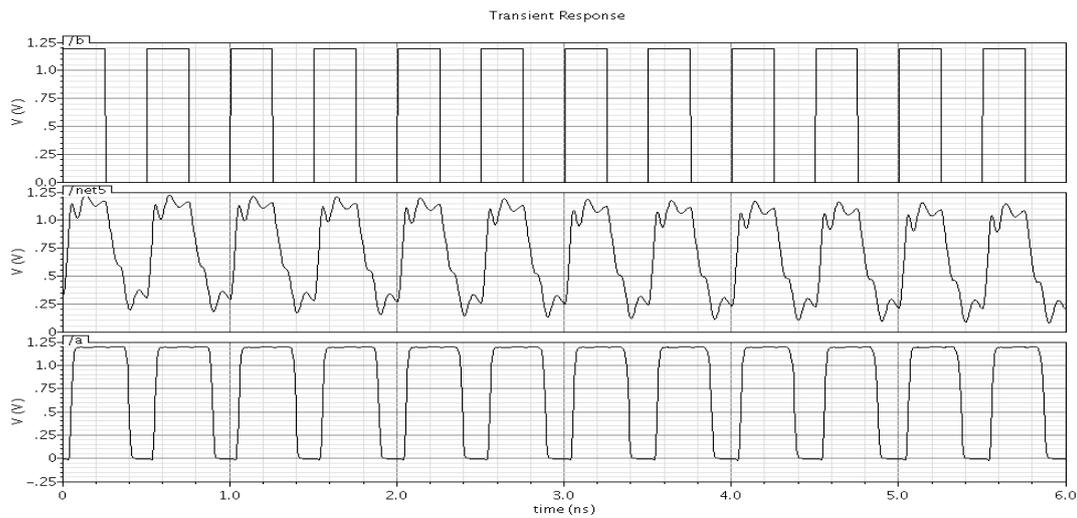


Figure 12. Bidirectional buffer inserted in RLC interconnect

It is observed that with buffer insertion in RLC signal has restored to great extent. Two parallel interconnects with coupling effects in between them are considered in Figure 13.

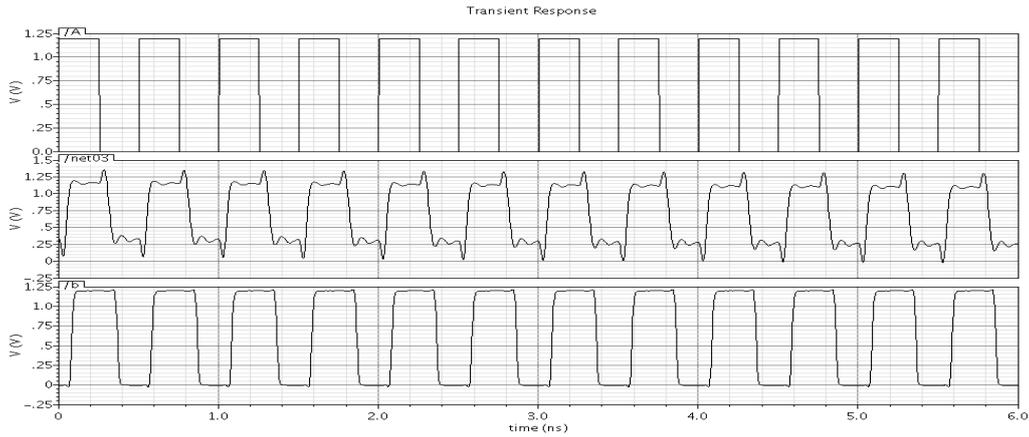


Figure 13. RLC coupling between interconnects

Due to coupling capacitance crosstalk is observed at the input of receiver driver. Shielding is done and crosstalk is reduced at the receiver driver node as in Figure 14.

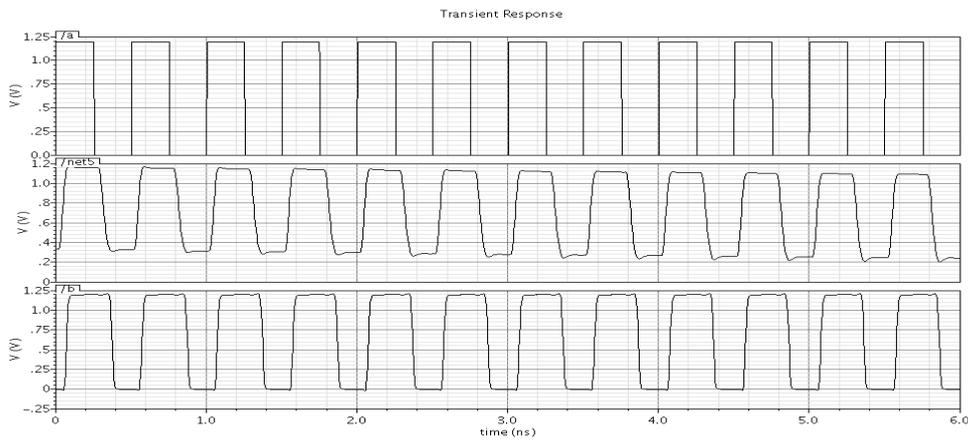


Figure 14. Shielding in interconnects

Skewing and shielding is done simultaneously and further reduction in crosstalk is observed as per waveform in Figure 15.

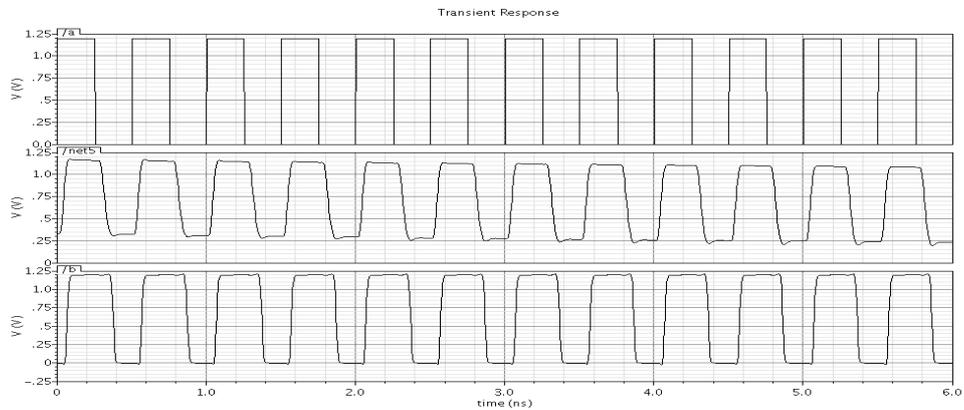


Figure 15. Skewing & Shielding in interconnects

The detailed analysis of crosstalk is done by calculating the maxima of signals at the input of the receiver buffer that being the critical node for the crosstalk observations. The propagation delay of RLC interconnect was found to be 129.6ps whereas with buffer insertion it reduced to 85.8ps.

Table below gives the different maxima values which in turn give us the crosstalk values achieved.

Direction of bidirectional buffer	At critical node	RLC coupling	shielding	skewing	Skewing + shielding
A to B	same	1.237 V	1.178V	1.196V	1.166V
	opposite	1.363V	1.179V	1.26V	1.169V
B to A	Same	1.236V	1.178V	1.20V	1.164V
	opposite	1.363V	1.179V	1.259V	1.169V

5. CONCLUSION

In order to reduce crosstalk noise, bidirectional buffer operating at 2GHz frequency is proposed along with buffer insertion and various techniques such as shielding, skewing so as to reduce the crosstalk noise. The proposed buffer also helped to reduce delay. It was observed that crosstalk noise is effectively reduced 57% with these techniques and delay is reduced by 34% with buffer insertion. Thus through the various results obtained using cadence at 90nm technology node we were able to analyze and reduce crosstalk through different techniques and by designing buffer operating at a higher frequency.

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